# UNITED STATES PATENT AND TRADEMARK OFFICE

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/043,047 | 01/09/2002 | Chang-Sik Yoo | SAM-0204 | 5014 |

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| 7590    07/21/2006 | EXAMINER |
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| Boston, MA  02108 | 2116 |

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 10/043,047 | YOO ET AL. |
| | Examiner | Art Unit | |
| | Tse Chen | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on <u>22 May 2006</u>.

2a) ☐ This action is **FINAL**.  2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) <u>54-56, 65-71, 73-80 and 87-114</u> is/are pending in the application.

    4a) Of the above claim(s) <u>72 and 81-86</u> is/are withdrawn from consideration.

5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.

6) ☒ Claim(s) <u>54-56, 65-71, 73-80 and 87-114</u> is/are rejected.

7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.

8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All  b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date \_\_\_\_\_.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. \_\_\_\_\_.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1.      A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on May 22, 2006 has been entered.

### *Election/Restrictions*

2.      Newly submitted claims 72, 81-86 are directed to an invention that is independent or

distinct from the invention originally claimed for the following reasons: claims 72, 81-86 are

directed to the original species concerning "memory system with claimed operations based on

both clock and flag signals" [Group A; pg.2 of paper 01052005] that has been canceled by

Applicant.

Since applicant has received an action on the merits for the originally presented

invention, this invention has been constructively elected by original presentation for prosecution

on the merits. Accordingly, claims 72, 81-86 are withdrawn from consideration as being

directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

### *Claim Rejections - 35 USC § 112*

3.      The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

4.     Claims 54-56 and 65 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to reasonably convey to one skilled in the

relevant art that the inventor(s), at the time the application was filed, had possession of the

claimed invention. Specifically, Applicant did not disclose "a second clock generator

independent of both the controller and the memory module for generating a second clock signal"

in the original disclosure. However, in the interest of compact prosecution, prior art is applied.

5.     The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the
> subject matter which the applicant regards as his invention.

6.     Claims 66-90, 106-109 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

7.     Where applicant acts as his or her own lexicographer to specifically define a term of a

claim contrary to its ordinary meaning, the written description must clearly redefine the claim

term and set forth the uncommon definition so as to put one reasonably skilled in the art on

notice that the applicant intended to so redefine that claim term. *Process Control Corp. v.*

*HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term

"buffer" in claims 66, 77-79, 106 is used by the claim to mean a module for "generating a second

clock signal", while the accepted meaning is "temporary storage"[1] [i.e., storages cannot generate

clock signals]. The term is indefinite because the specification does not clearly redefine the term.

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[1] Newton's Telecom Dictionary, pg. 135 under "buffer".

However, in the interest of compact prosecution, Examiner will take the position that the claimed

"control/address buffer" is a control address *module* capable of storing and generating signals.

### *Claim Rejections - 35 USC § 102*

8.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9.       Claims 54-56, 65-67, 73-79, 91, 93-96, 101-104, 106, 107, 109, 110, 112-114 are rejected

under 35 U.S.C. 102(e) as being anticipated by Gillingham et al., US Patent 6510503, hereinafter

Gillingham.

10.     In re claim 54, Gillingham discloses a memory system [80] having a stub configuration

[col.10, l.58 – col.11, l.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [col/row], an

  address signal [col.3, ll.1-12] and data signals on a data bus, the data bus, first clock

  signal, control signal, and address signal being arranged in a stub configuration [col.10,

  l.10 – col.11, l.8; col.12, ll.1-12; fig.7].

- A memory module [170] including memory devices [100, 174] coupled to the controller.

- A second clock signal generator [107, 108 with associated components such as muxes

  and buffers] independent of both the controller and the memory module [independent

  delays] for generating a second clock signal [outclk, dclk] [col.10, 40-45; col.11, ll.23-

  49].

- The memory module receiving the first clock signal, the second clock signal and the control signal that includes a read or write command [col.2, ll.16-47; col.10, ll.10-23; col.11, ll.23-49; fig.13, 14].

- The first clock signal propagating from the controller to the memory module in a first direction of propagation, and the second clock signal propagating from the memory module to the controller in a second direction of propagation [col.10, ll.10-23, ll.49-53; col.11, ll.23-49; 86 propagates from controller to module and dclk propagates from module to controller in a read operation].

- The memory module, in response to the write command, initiating a write operation for writing the data signals from the data bus to the memory devices in synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].

- The memory module, in response to the read command, initiating a read operation for reading data from the memory devices to the data bus in response to the second clock signal, the controller receiving the data signals on the data bus in response to the second clock signal during the read operation [col.11, ll.23-49].

11.     As to claims 55, 73, 101, Gillingham discloses, wherein the first clock signal comprises a write clock and wherein the second clock signal comprises a read clock [col.10, ll.49-53; col.11, ll.23-49].

12.     As to claim 56, Gillingham discloses, wherein the memory controller further compensates for phase difference between the received second clock signal and the data signals on the data bus [col.13, ll.20-37].

13.    In re claim 65, Gillingham discloses each and every limitation as discussed above in

reference to claim 54. Gillingham discloses the memory system; therefore, Gillingham discloses

the method of operating the memory system.

14.    In re claim 66, Gillingham discloses a memory system [80] having a stub configuration

[col.10, 1.58 – col.11, 1.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [e.g., row], an

    address signal [e.g., col] [col.3, ll.1-12] and data signals on a first clock signal line, a

    control signal line, and address signal line and a data bus, respectively [col.10, 1.10 –

    col.11, 1.8; col.12, ll.1-12; fig.7].

- A first memory module [170] including at least one memory device [100, 174] connected

    to the data bus and the first clock signal line for receiving the data signals and the first

    clock signal respectively, and a control/address module [106, 107, 108 with associated

    circuitry] that is connected to the control signal line, the address signal line and the first

    clock signal line for receiving the control signal, the address signal, and the first clock

    signal respectively [fig.8a].

- The first memory module, in response to the write command, initiating a write operation

    for writing the data signals from the data bus to the at least one memory device in

    synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].

- The first memory module, in response to the read command, initiating a read operation

    for reading data from the at least one memory device to the data bus, and the

    control/address module generating a second clock signal [outclk, dclk] in response to the

    first clock signal, the second clock signal being provided to the controller on a second

clock signal line that is separate from the first clock signal line [86, clk propagates from

controller to module and dclk propagates from module to controller in a read operation],

the controller receiving the data signals on the data bus in response to the second clock

signal during the read operation [col.10, ll.40-57; col.11, ll.23-49].

15.      As to claims 67, 96, 107, Gillingham discloses, wherein the memory system further

includes a second memory module, the first and second memory modules generating respective

first and second independent return clock signals as the second clock signal [170 corresponds to

84 each with its own clock generators of dclk], and further comprising a motherboard coupling

the first and second memory modules and the controller, the motherboard including the data bus,

the control signal line, the address signal line, the first clock signal line and first and second

independent return clock signal lines for transfer of the first and second return clock signals form

the first and second memory modules to the controller [fig.7, 8a, 8c, 13].

16.      As to claims 74, 102, 109, Gillingham discloses, wherein the system comprises multiple

memory modules and wherein the multiple memory modules each generate independent second

clock signals, the second clock each being different in phase relative to each other [col.13, ll.39-

54; phase differences require synchronization].

17.      As to claims 75, 103, Gillingham discloses, wherein the phases of the multiple second

clock signals are different in phase due to the difference in propagation delay between each of

the memory modules and the controller [col.2, ll.42-44, ll.59-60; memory modules situated at

different distances induce different propagation delays].

18. As to claims 76, 104, Gillingham discloses, wherein the propagation delay of the second clock signal on the second clock signal line from the first memory module to the controller is substantially equal to that of the data signals on the data bus [col.2, ll.36-38].

19. As to claims 77, 94, 113, Gillingham discloses, wherein the control/address module or clock return further includes a phase locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal [col.2, ll.10-13].

20. As to claims 78, 95, 114, Gillingham discloses, wherein the control/address module or clock return further includes a delay locked loop that receives the first clock signal and generates the second clock signal in response to the first clock signal [col.2, ll.10-13].

21. As to claim 79, Gillingham discloses, wherein the control/address module includes a return path that is coupled to a first clock signal line that receives the first clock signal for generating the second clock signal in response to the first clock signal [fig.6a; cfc loops to ctc].

22. In re claim 91, Gillingham discloses a memory system [80] having a stub configuration [col.10, l.58 – col.11, l.8] comprising:

- A controller [82] for generating a first clock signal [86], a control signal [e.g., row], an address signal [e.g., col] [col.3, ll.1-12] and data signals on a first clock signal line, a control signal line, and address signal line and a data bus, respectively [col.10, l.10 – col.11, l.8; col.12, ll.1-12; fig.7].

- A first memory module [170] including at least one memory device [100, 174] connected to the data bus and the first clock signal line for receiving the data signals and the first clock signal respectively, and a clock return [106, 107, 108 with associated circuitry] that is coupled to the first clock signal line that receives first clock signal [fig.8a].

- The first memory module, in response to the write command, initiating a write operation

    for writing the data signals from the data bus to the at least one memory device in

    synchronization with the first clock signal [col.10, ll.49-53; uses 86 to write data].

- The first memory module, in response to the read command, initiating a read operation

    for reading data from the at least one memory device to the data bus, and the clock return

    providing a second clock signal [outclk, dclk] in response to the first clock signal, the

    second clock signal being provided to the controller on a second clock signal line that is

    separate from the first clock signal line [86, clk propagates from controller to module and

    dclk propagates from module to controller in a read operation], the controller receiving

    the data signals on the data bus in response to the second clock signal during the read

    operation [col.10, ll.40-57; col.11, ll.23-49].

23.     As to claims 93, 112, Gillingham discloses, wherein the first memory module further

includes a control/address buffer [106] that is connected to the control signal line, the address

signal line and the first clock signal line for receiving the control signal, the address signal, and

the first clock signal [fig.8a].

24.     In re claim 106, Gillingham discloses each and every limitation as discussed above in

reference to claim 66. Gillingham discloses the memory system; therefore, Gillingham discloses

the method of operating the memory system.

25.     In re claim 110, Gillingham discloses each and every limitation as discussed above in

reference to claim 91. Gillingham discloses the memory system; therefore, Gillingham discloses

the method of operating the memory system.

*Claim Rejections - 35 USC § 103*

26.     The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

27.     Claims 68, 97, 108 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gillingham as applied to claims 67, 96, 107 above, and further in view of Wada et al., US Patent

5379248, hereinafter Wada.

28.     Gillingham taught each and every limitation as discussed above. Gillingham did not

disclose explicitly that the first and second return clock signal lines are crossed on the

motherboard between the first and second modules.

29.     Wada discloses a memory system wherein a first and second signal lines [bit lines] are

crossed between a first and second modules [peripheral circuits] [abstract].

30.     It would have been obvious to one of ordinary skill in the art, having the teachings of

Gillingham and Wada before him at the time the invention was made, to modify the memory

system taught by Gillingham to include the teachings of Wada, in order to obtain the memory

system wherein the first and second return clock signal lines are crossed on the motherboard

between the first and second modules. One of ordinary skill in the art would have been motivated

to make such a combination as it provides a way to increase the freedom of circuit line layout

[Wada: abstract].

31.     Claims 69-71, 87-89, 98-100 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Gillingham as applied to claims 11and 66 above, and further in view of Yoshitake, US

Patent 6043704.

32.    Gillingham taught each and every limitation as discussed above. Gillingham did not

discuss the details of a dummy load regarding the memory modules [Gillingham: col.13, ll.20-

37; col.15, 1.60 – col.16, 1.46].

33.    In re claims 69 and 98, Yoshitake discloses a system wherein a return clock signal line

[clock wiring line] is coupled to a dummy load [31] [col.10, ll.56-64].

34.    It would have been obvious to one of ordinary skill in the art, having the teachings of

Gillingham and Yoshitake before him at the time the invention was made, to modify the memory

system taught by Gillingham to include the teachings of Yoshitake, in order to obtain the

memory system wherein the first return clock signal line is coupled to a dummy load on the

second memory module and wherein the second return clock signal line is coupled to a dummy

load on the first memory module. One of ordinary skill in the art would have been motivated to

make such a combination as it provides a very well known way to correct clock skews

[Yoshitake: col.10, ll.56-64] and match input capacitance [Gillingham: col.13, ll.20-37].

35.    As to claims 70, 88, 99, Yoshitake discloses, wherein the dummy load comprises a load

capacitor or a dummy pin [col.10, ll.56-64; 31 contains capacitance load].

36.    As to claims 71, 100, Yoshitake discloses, wherein the dummy load is selected to match

the capacitance loading of a data bus [multiple clock wiring lines constitute a bus as is well

known in the art] [col.10, ll.56-64; 31 adjusted to match capacitance in order to adjust skew].

37.    As to claim 87, Yoshitake discloses, comprising a module [second buffers] mounted to a

first side of a memory module [10 contains RAM], and further comprising a dummy load [31]

for coupling to a first signal line of the module to provide load matching with a load experienced

by a second signal line of memory devices [third buffers] mounted to both first and second sides

of the memory module [col.3, 1.54 – col.5, 1.63; col.10, 11.56-64].

38.     As to claim 89, Yoshitake discloses, wherein the first signal line comprises the first clock

signal line or the second clock signal line, and wherein the second signal line comprises the data

bus or the first clock signal line [col.3, 1.54 – col.5, 1.63; col.10, 11.56-64].

39.     Claims 80, 92, 111 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gillingham as applied to claims 79, 91, 110 above, and further in view of Moyal et al., US Patent

6326853, hereinafter Moyal.

40.     Gillingham taught each and every limitation as discussed above in reference to claim 9.

Gillingham did not discuss the details of the memory module regarding capacitors.

41.     Moyal discloses a system comprising a capacitor having a capacitance that is selected to

compensate for capacitive loading; the capacitor being coupled to a junction of a signal line and

a return path [fig.4; col.2, 11.1-11].

42.     It would have been obvious to one of ordinary skill in the art, having the teachings of

Gillingham and Moyal before him at the time the invention was made, to modify the memory

system taught by Gillingham to include the teachings of Moyal, in order to obtain the memory

system wherein the memory module further includes a capacitor having a capacitance that is

selected to compensate for capacitive loading on the data bus by the memory device of the

memory module; the capacitor being coupled to a junction of the first clock signal line and the

return path. One of ordinary skill in the art would have been motivated to make such a

combination as it provides a way to reduce phase mismatches [Moyal: col.2, 11.1-11].

43.    Claims 90, 105 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Gillingham as applied to claim 66 above, and further in view of Keeth, US Patent 6029250.

44.    Gillingham taught each and every limitation as discussed above. Gillingham did not

discuss the details of clock generations in the memory module.

45.    Keeth discloses a memory system [fig.4] comprising a memory module [404], in

response to a read command, initiating a read operation for reading data from memory devices

[80a-h] to a data bus [dq] in synchronization with a first clock signal [rclk] and generating a

second clock signal [dclk0/1] in response to the first clock signal, the data signals and the second

clock signal being output from the memory module in synchronization with the first clock signal

[fig.5; dclk in sync with rclk; data in sync with dclk in order to be latched correctly], the second

clock signal being provided to a controller [402], the controller receiving the data signals on the

data bus in response to the second clock signal during the read operation [col.10, ll.26-39; col.13,

ll.8-23, l.40 – col.15, l.14].

46.    It would have been obvious to one of ordinary skill in the art, having the teachings of

Gillingham and Keeth before him at the time the invention was made, to modify the memory

module taught by Gillingham to include the teachings of Keeth, in order to obtain the memory

system comprising during the read operation, the data signals and the second clock signal are

output from the first memory module in synchronization with the first clock signal. One of

ordinary skill in the art would have been motivated to make such a combination as it provides a

way to better synchronize memory access of increasing number of memory modules [Keeth:

col.1, l.17 – col.2, l.14; col.7, ll.28-52].

*Response to Arguments*

47.    Applicant's arguments with respect to claim May 22, 2006 have been considered but are

moot in view of the new ground(s) of rejection.

*Conclusion*

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The

examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Tse Chen
June 27, 2006